

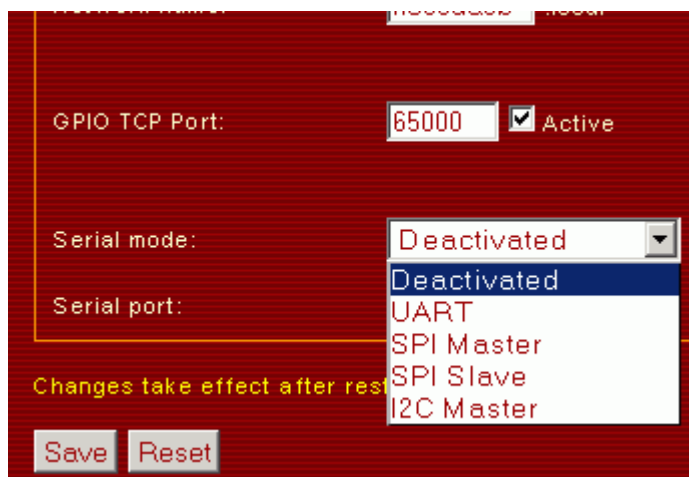
# Serial server

Using the serial server, access to different serial interfaces is possible via a TCP/IP-connection.

Since **version 1.2**, the following interfaces are supported:

- Asynchronous serial interace full-duplex - [UART](#)
- Synchronous serial interface full-duplex - [SPI Master](#)
- TCP/IP - modem at synchronous serial interface half-duplex - [SPI Slave](#)
- Two-Wire interface- [I2C Master](#)

Since **version 1.5pro** the [I2C Monitor](#) mode is supported.



The interface as well as the TCP/IP-port of the serial server are set on the website with the general settings. The new settings always become only active after restart of the Netzer.

The interfaces occupy different [IOs](#) of the Netzer. A free configuration of those is then not possible from the [GPIO-main page](#).

Apart from the TCP/IP-modem, all modes are structures that way that after restart Netzer opens a socket with a correspondingly configured port and listens to incoming connections.

Once a connection is made, it is then possible to directly send data to the respective serial interface and received by it as well. Depending on the chosen interface, a certain protocol overhead is still required to be transferred.

A receive buffer and a send buffer are interposed between the TCP/IP-socket. Both buffers have 256 byte. All data communication is done via these buffers to increase the data throughput on the serial interfaces.

## Settings

SYSTEM STATE

COMMON

GPIO

• SERIAL

UART settings

UART Baudrate: 19200 Baud

Common SPI settings (SPI Slave: Changes take effect after restart)

Clock mode:

- SPI Mode 0
- SPI Mode 1
- SPI Mode 2
- SPI Mode 3

SPI Master settings

Clock frequency: 10.4 MBit/s

Input sampling:

- At middle of data output
- At end of data output

I2C Master settings (SCL = SPI\_CLK, SDA = SPI\_MI)

Clock frequency: 400 kHz

Save Reset

## SPI

For SPI, particularly the clock mode is important. The setting applies likewise to Master and Slave. It defines the polarity of the clock signal as well as the transfer edge as follows:

Mode	Idle mode of the clock signal	transfer edge
Mode 0	0	rising
Mode 1	0	falling
Mode 2	1	falling
Mode 3	1	rising



For the successful data transfer, the modes of Master and Slave should be equivalent!

Amendments of this setting at the SPI-slave become effective after restart only.



In SPI-slave mode it is important that the Master actually creates the set resting potential for the clock signal at the beginning, since otherwise the Netzer may not activate the SPI-module!

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